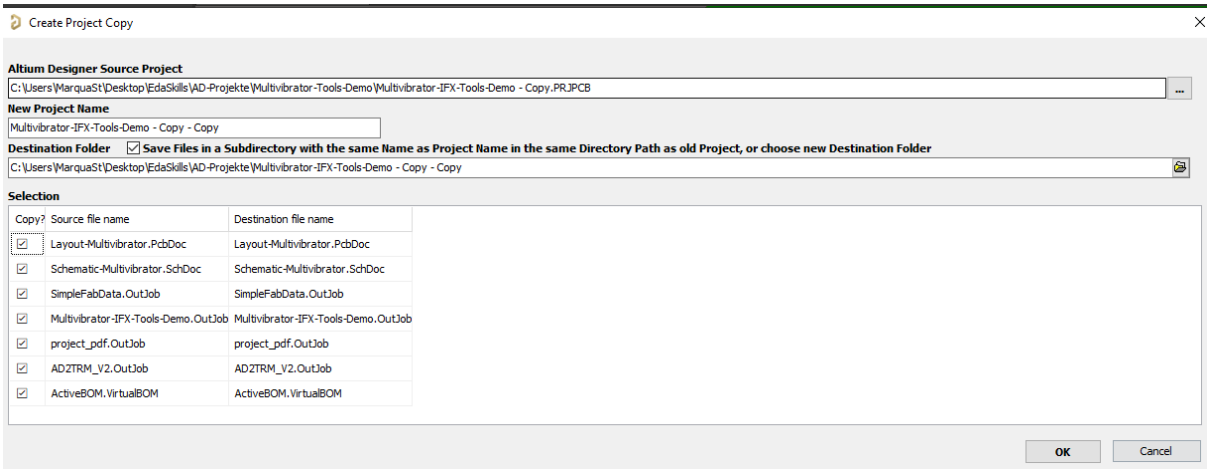
Inhalt

Altium Designer

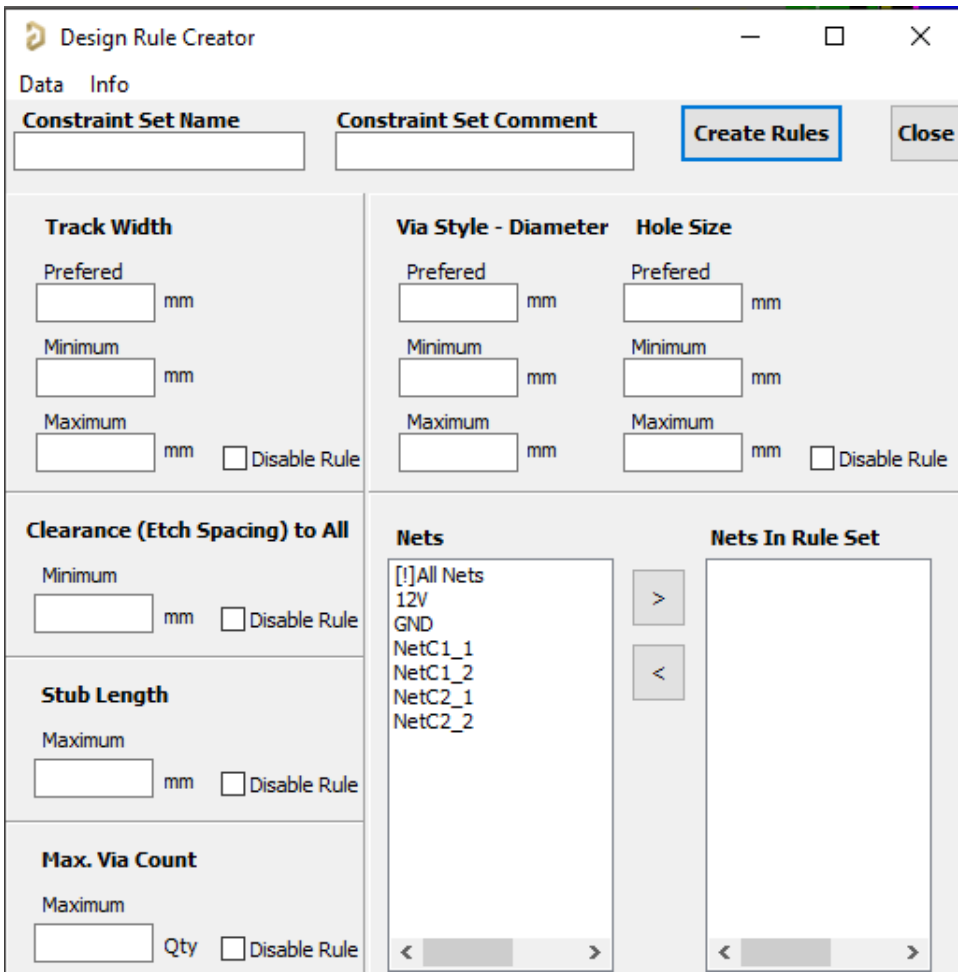
Clone Project

Ein Skript zum Kopieren von Projekten.



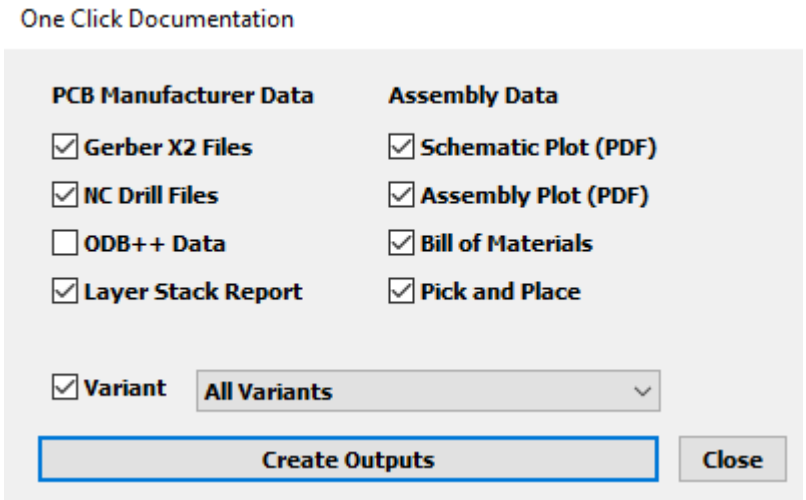
Design Rule Creator

Skript zum schnellen Erstellen von einfachen Regeln für den Design Rule Check.



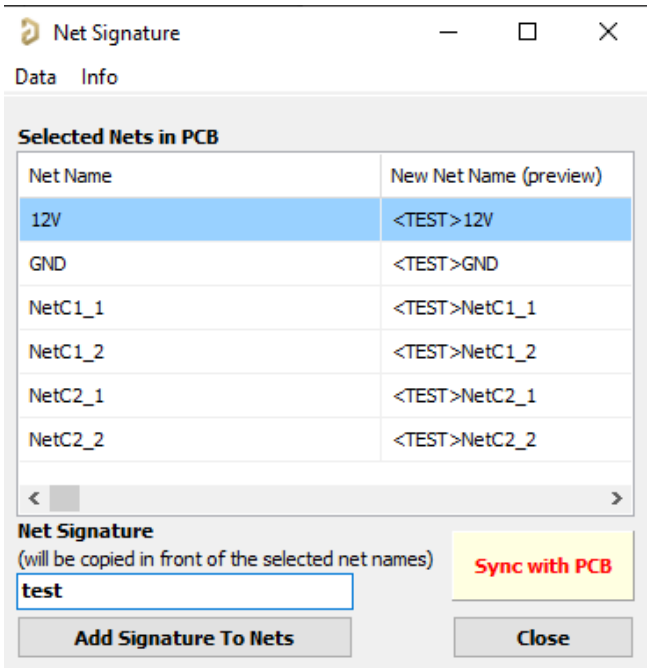
One Click Documentation

Das Skript erstellt die komplette Fertigungsdaten und Dokumentation zu einer bestückten Leiterplatte.



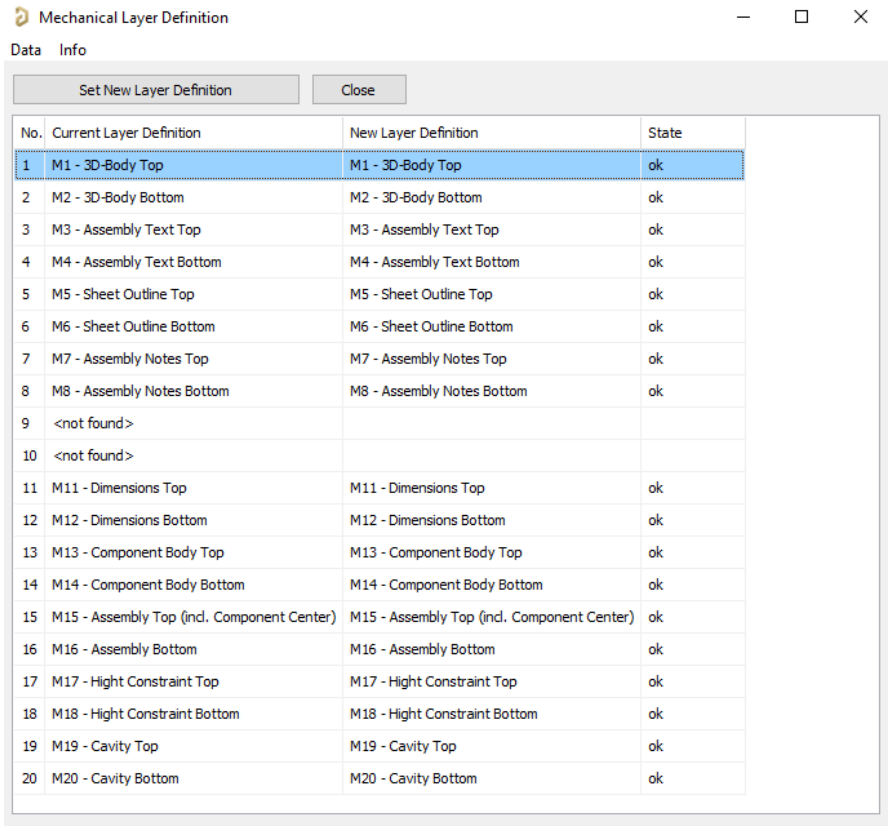
Net Signature

Mit diesem Skript können Netznamen individuell erweitert werden.



Mechanical Layer Definition

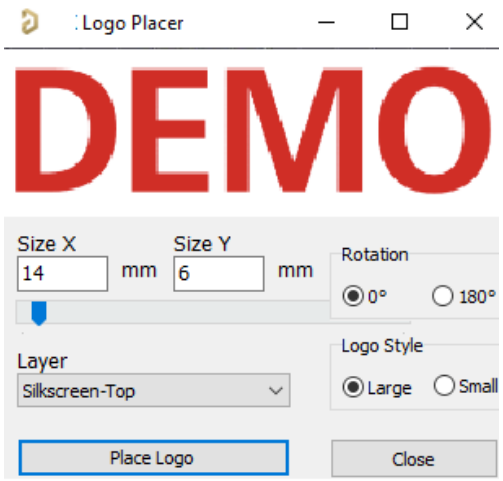
Skript setzt die Namen der mechanischen Lagen eines PCB zu einem definierten Standard.



No.	Current Layer Definition	New Layer Definition	State
1	M1 - 3D-Body Top	M1 - 3D-Body Top	ok
2	M2 - 3D-Body Bottom	M2 - 3D-Body Bottom	ok
3	M3 - Assembly Text Top	M3 - Assembly Text Top	ok
4	M4 - Assembly Text Bottom	M4 - Assembly Text Bottom	ok
5	M5 - Sheet Outline Top	M5 - Sheet Outline Top	ok
6	M6 - Sheet Outline Bottom	M6 - Sheet Outline Bottom	ok
7	M7 - Assembly Notes Top	M7 - Assembly Notes Top	ok
8	M8 - Assembly Notes Bottom	M8 - Assembly Notes Bottom	ok
9	<not found>		
10	<not found>		
11	M11 - Dimensions Top	M11 - Dimensions Top	ok
12	M12 - Dimensions Bottom	M12 - Dimensions Bottom	ok
13	M13 - Component Body Top	M13 - Component Body Top	ok
14	M14 - Component Body Bottom	M14 - Component Body Bottom	ok
15	M15 - Assembly Top (incl. Component Center)	M15 - Assembly Top (incl. Component Center)	ok
16	M16 - Assembly Bottom	M16 - Assembly Bottom	ok
17	M17 - Hight Constraint Top	M17 - Hight Constraint Top	ok
18	M18 - Hight Constraint Bottom	M18 - Hight Constraint Bottom	ok
19	M19 - Cavity Top	M19 - Cavity Top	ok
20	M20 - Cavity Bottom	M20 - Cavity Bottom	ok

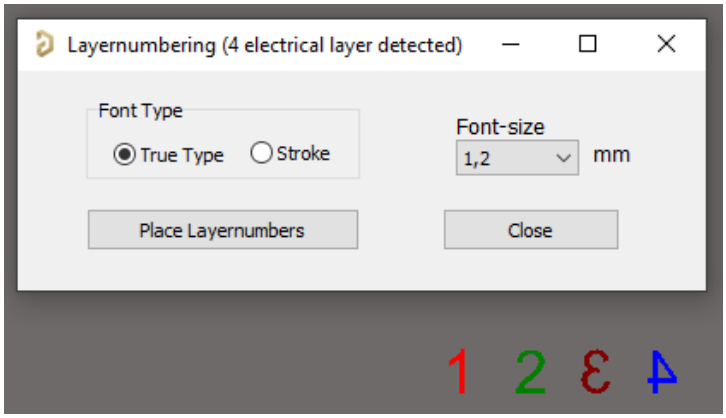
Logo Placer

Mit diesem Skript können auf Bitmaps basierende Bilder als PCB-Logos platziert werden.



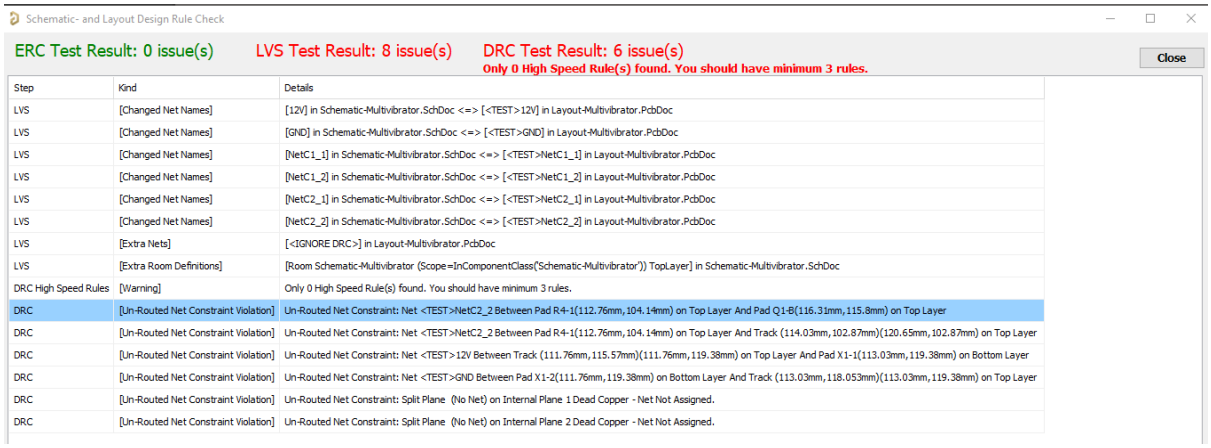
Layer Numbering

Das Skript setzt einen PCB-String mit der entsprechenden Lagennummer auf die elekrischen Lagen.



Schematic- and Layout Design Rule Check

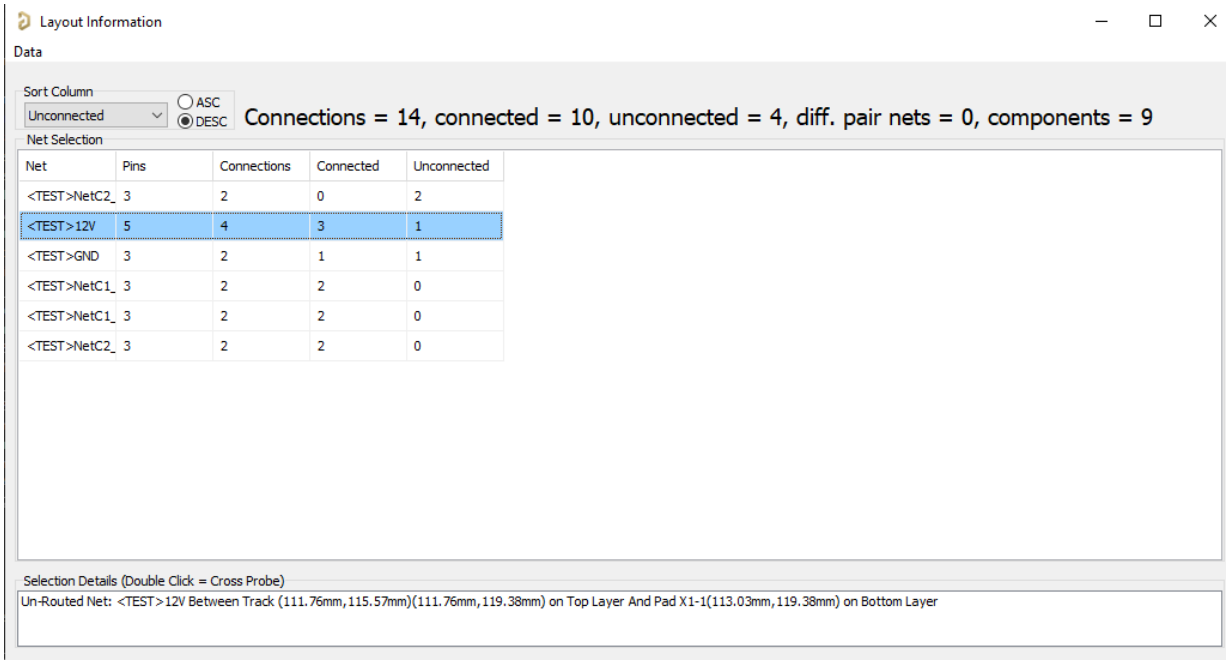
Das Skript steuert verschiedene Testläufe und ordnet die Ergebnisse zu einem strukturierten Report.



Step	Kind	Details
LVS	[Changed Net Names]	[12V] in Schematic-Multivibrator.SchDoc <=> [<TEST>12V] in Layout-Multivibrator.PcbDoc
LVS	[Changed Net Names]	[GND] in Schematic-Multivibrator.SchDoc <=> [<TEST>GND] in Layout-Multivibrator.PcbDoc
LVS	[Changed Net Names]	[NetC1_1] in Schematic-Multivibrator.SchDoc <=> [<TEST>NetC1_1] in Layout-Multivibrator.PcbDoc
LVS	[Changed Net Names]	[NetC1_2] in Schematic-Multivibrator.SchDoc <=> [<TEST>NetC1_2] in Layout-Multivibrator.PcbDoc
LVS	[Changed Net Names]	[NetC2_1] in Schematic-Multivibrator.SchDoc <=> [<TEST>NetC2_1] in Layout-Multivibrator.PcbDoc
LVS	[Changed Net Names]	[NetC2_2] in Schematic-Multivibrator.SchDoc <=> [<TEST>NetC2_2] in Layout-Multivibrator.PcbDoc
LVS	[Extra Nets]	[<IGNORE DRC>] in Layout-Multivibrator.PcbDoc
LVS	[Extra Room Definitions]	[Room Schematic-Multivibrator (Scope=InComponentClass('Schematic-Multivibrator')) TopLayer] in Schematic-Multivibrator.SchDoc
DRC High Speed Rules	[Warning]	Only 0 High Speed Rule(s) found. You should have minimum 3 rules.
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Net <TEST>NetC2_2 Between Pad R4-1(112.76mm,104.14mm) on Top Layer And Pad Q1-B(116.31mm,115.8mm) on Top Layer
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Net <TEST>NetC2_2 Between Pad R4-1(112.76mm,104.14mm) on Top Layer And Track (114.03mm,102.87mm)(120.65mm,102.87mm) on Top Layer
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Net <TEST>12V Between Track (111.76mm,115.57mm)(111.76mm,119.38mm) on Top Layer And Pad X1-1(113.03mm,119.38mm) on Bottom Layer
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Net <TEST>GND Between Pad X1-2(111.76mm,119.38mm) on Bottom Layer And Track (113.03mm,118.053mm)(113.03mm,119.38mm) on Top Layer
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Split Plane (No Net) on Internal Plane 1 Dead Copper - Net Not Assigned.
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Split Plane (No Net) on Internal Plane 2 Dead Copper - Net Not Assigned.

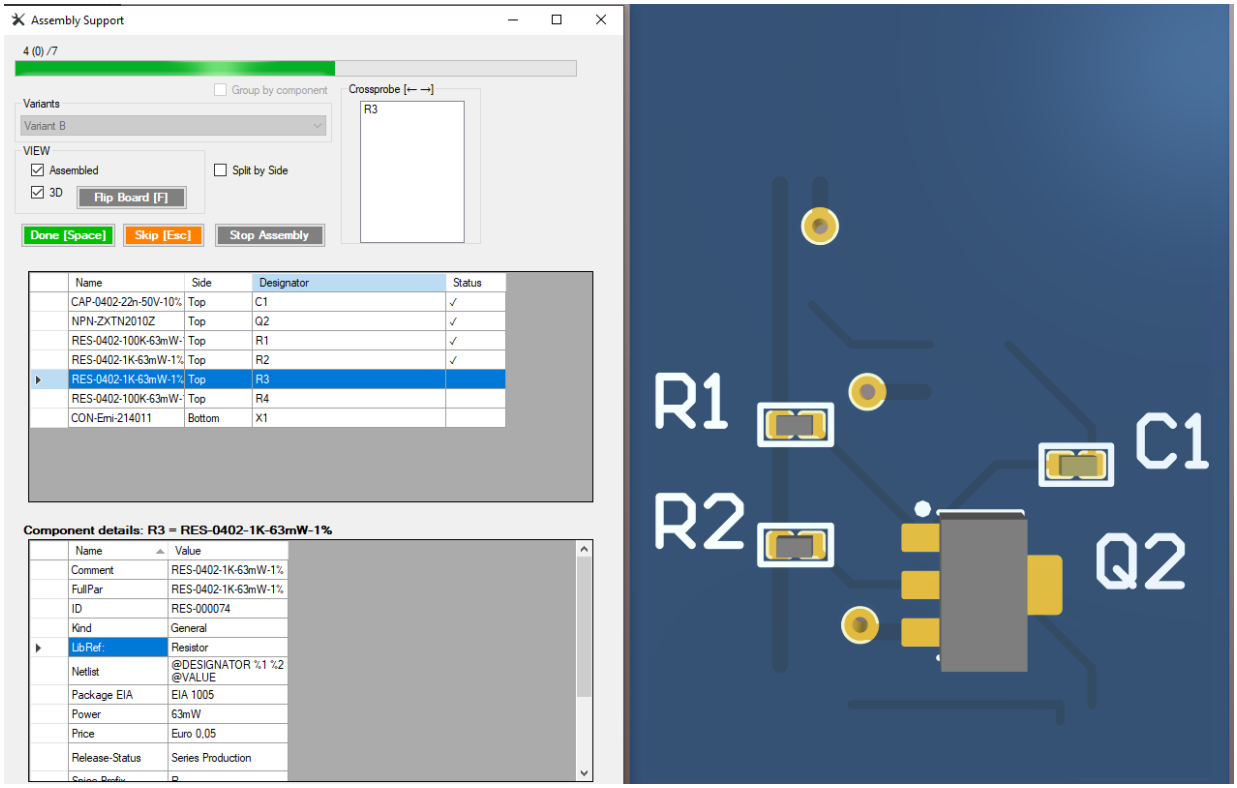
Layout Information

Das Skript erstellt einen Bericht zu dem Layoutzustandes des PCB.



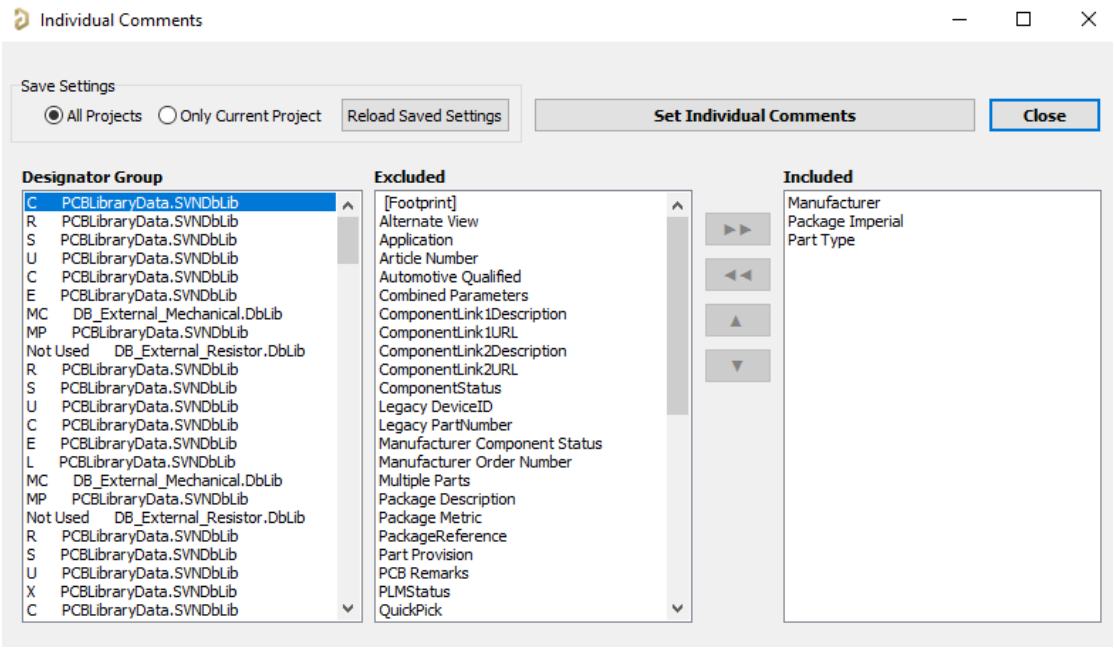
Assembly Support

Mit diesem Skript wird man bei handbestückten PCB's bei der Bestückung assistiert. Die Bauteile können per Crossprobing ermittelt- und als bestückt signiert werden.



Individual Comments

Mit diesem Skript können die PCB-Kommentare entsprechend der Bauteilklasse zusammengestellt werden.



Allegro

One Click Documentaion

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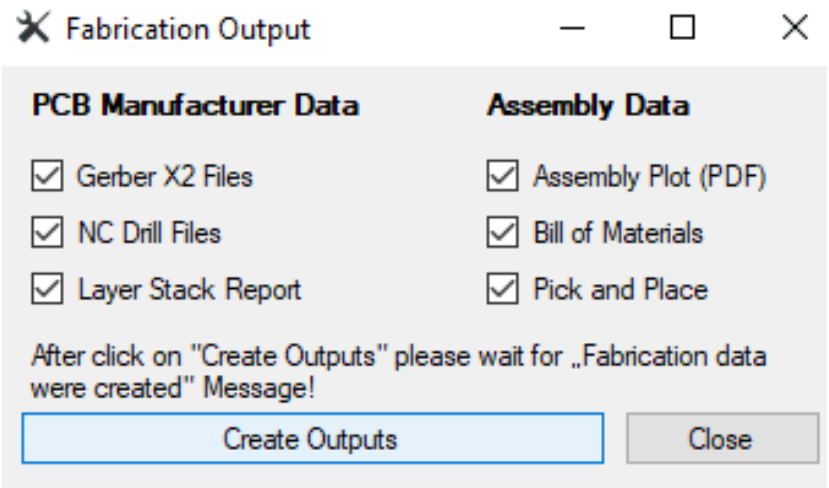

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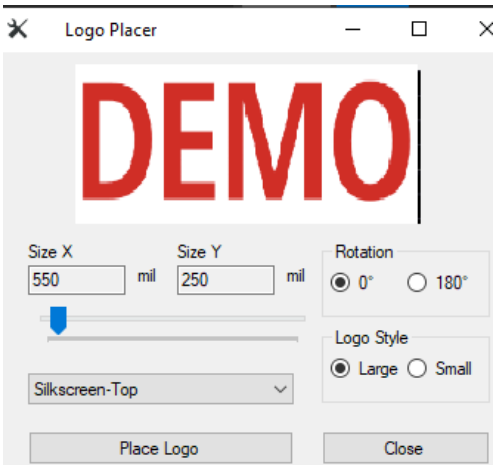

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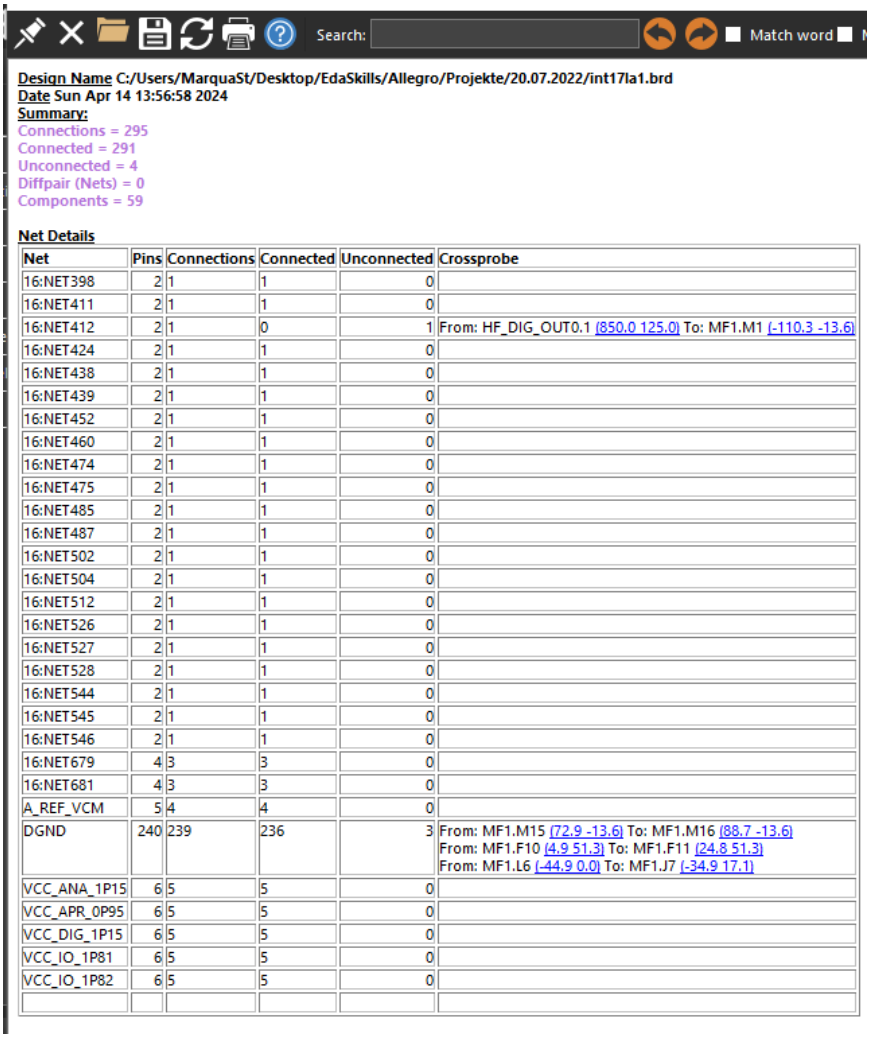

Design Name C:/Users/MarquaSt/Desktop/EdaSkills/Allegro/Projekte/20.07.2022/int17la1.brd
Date Sun Apr 14 13:56:58 2024
Summary:
Connections = 295
Connected = 291
Unconnected = 4
Diffpair (Nets) = 0
Components = 59

Net Details

Net	Pins	Connections	Connected	Unconnected	Crossprobe
16:NET398	2	1	1	0	
16:NET411	2	1	1	0	
16:NET412	2	1	0	1	From: HF_DIG_OUT0.1 (850.0 125.0) To: MF1.M1 (-110.3 -13.6)
16:NET424	2	1	1	0	
16:NET438	2	1	1	0	
16:NET439	2	1	1	0	
16:NET452	2	1	1	0	
16:NET460	2	1	1	0	
16:NET474	2	1	1	0	
16:NET475	2	1	1	0	
16:NET485	2	1	1	0	
16:NET487	2	1	1	0	
16:NET502	2	1	1	0	
16:NET504	2	1	1	0	
16:NET512	2	1	1	0	
16:NET526	2	1	1	0	
16:NET527	2	1	1	0	
16:NET528	2	1	1	0	
16:NET544	2	1	1	0	
16:NET545	2	1	1	0	
16:NET546	2	1	1	0	
16:NET679	4	3	3	0	
16:NET681	4	3	3	0	
A_REF_VCM	5	4	4	0	
DGND	240	239	236	3	From: MF1.M15 (72.9 -13.6) To: MF1.M16 (88.7 -13.6) From: MF1.F10 (4.9 51.3) To: MF1.F11 (24.8 51.3) From: MF1.L6 (-44.9 0.0) To: MF1.J7 (-34.9 17.1)
VCC_ANA_1P15	6	5	5	0	
VCC_APR_0P95	6	5	5	0	
VCC_DIG_1P15	6	5	5	0	
VCC_IO_1P81	6	5	5	0	
VCC_IO_1P82	6	5	5	0	