

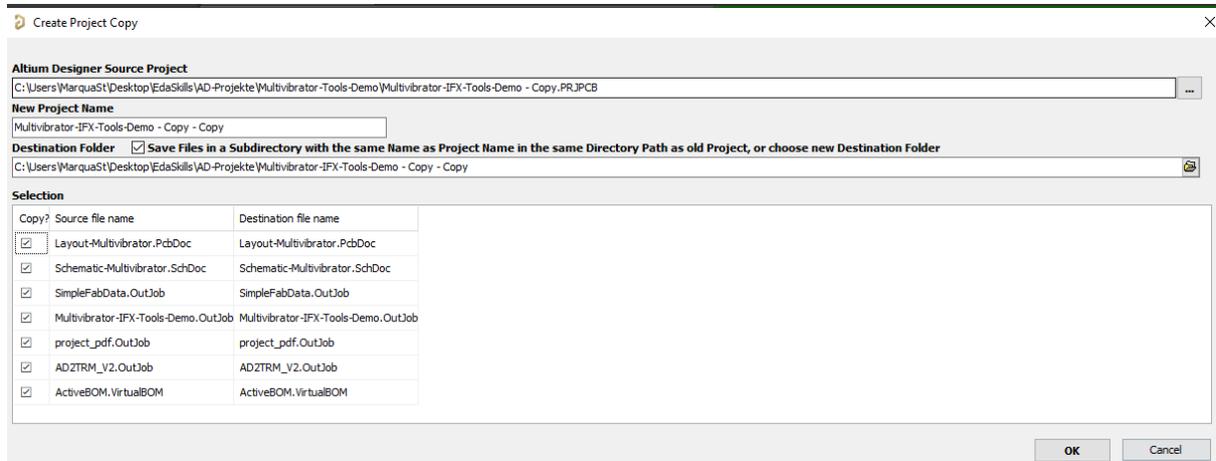
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## Altium Designer

### Clone Project

Ein Skript zum Kopieren von Projekten.



## Design Rule Creator

Skript zum schnellen Erstellen von einfachen Regeln für den Design Rule Check.

The screenshot shows the 'Design Rule Creator' dialog box with the following sections:

- Constraint Set Name:** An empty text input field.
- Constraint Set Comment:** An empty text input field.
- Create Rules:** A button highlighted with a blue border.
- Close:** A button.
- Track Width:** Three input fields for 'Preferred', 'Minimum', and 'Maximum' (all in mm), and a 'Disable Rule' checkbox.
- Via Style - Diameter:** Three input fields for 'Preferred', 'Minimum', and 'Maximum' (all in mm), and a 'Disable Rule' checkbox.
- Hole Size:** Three input fields for 'Preferred', 'Minimum', and 'Maximum' (all in mm), and a 'Disable Rule' checkbox.
- Clearance (Etch Spacing) to All:** One input field for 'Minimum' (in mm) and a 'Disable Rule' checkbox.
- Stub Length:** One input field for 'Maximum' (in mm) and a 'Disable Rule' checkbox.
- Max. Via Count:** One input field for 'Maximum' (in Qty) and a 'Disable Rule' checkbox.
- Nets:** A list box containing: [!]All Nets, 12V, GND, NetC1\_1, NetC1\_2, NetC2\_1, NetC2\_2.
- Nets In Rule Set:** An empty list box.
- Navigation arrows (> and <) are located between the 'Nets' and 'Nets In Rule Set' list boxes.

## One Click Documentation

Das Skript erstellt die komplette Fertigungsdaten und Dokumentation zu einer bestückten Leiterplatte.

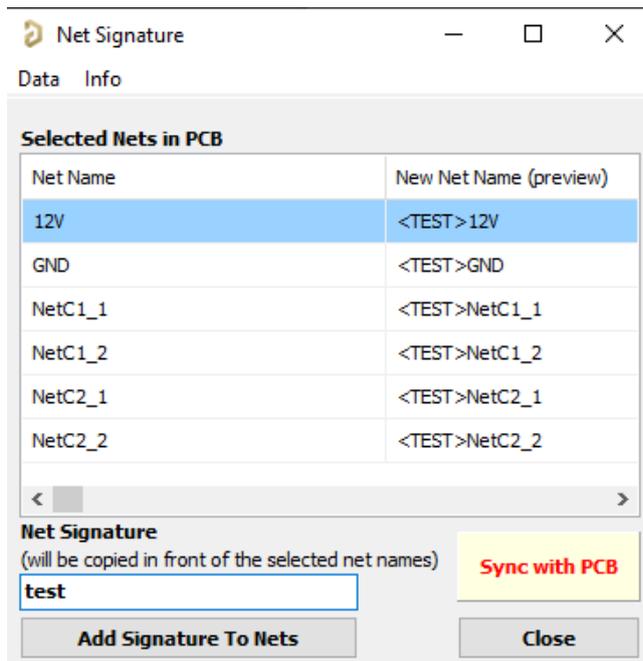
### One Click Documentation

The screenshot shows the 'One Click Documentation' dialog box with the following sections:

- PCB Manufacturer Data:**
  - Gerber X2 Files
  - NC Drill Files
  - ODB++ Data
  - Layer Stack Report
- Assembly Data:**
  - Schematic Plot (PDF)
  - Assembly Plot (PDF)
  - Bill of Materials
  - Pick and Place
- Variant:**  Variant, with a dropdown menu set to 'All Variants'.
- Create Outputs:** A button highlighted with a blue border.
- Close:** A button.

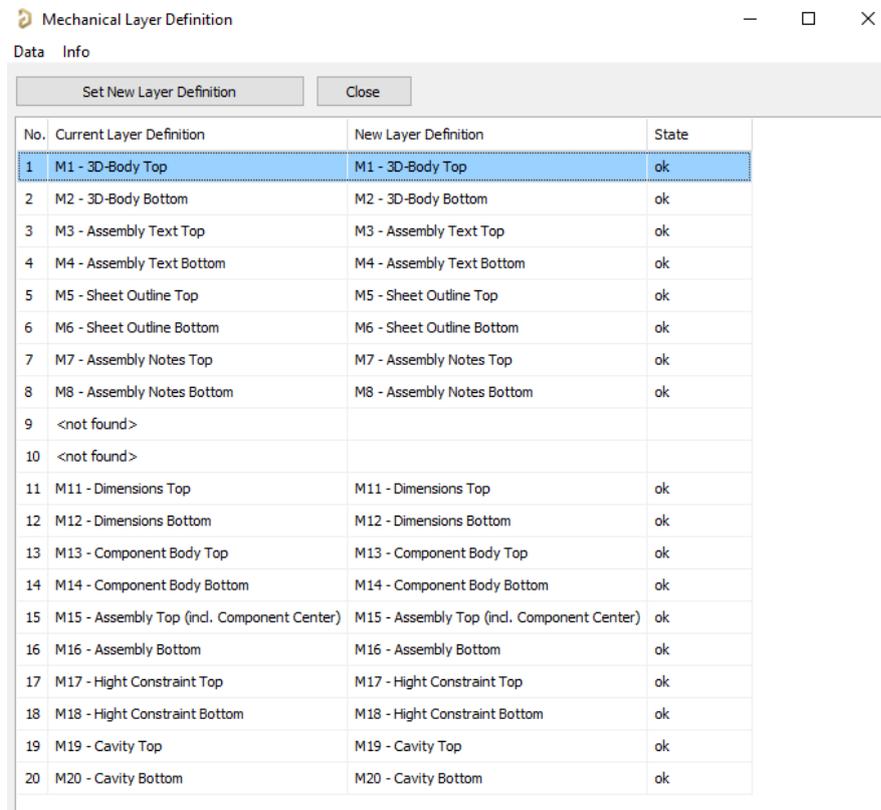
## Net Signature

Mit diesem Skript können Netznamen individuell erweitert werden.



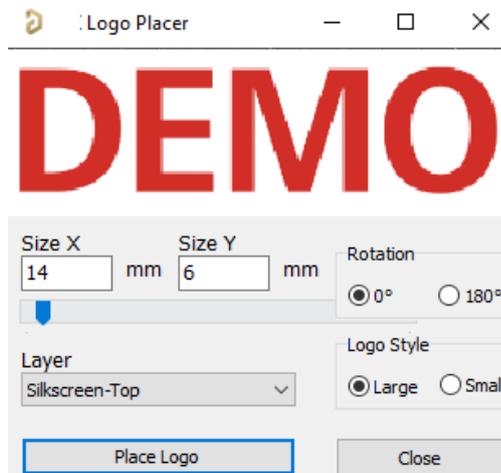
## Mechanical Layer Definition

Skript setzt die Namen der mechanischen Lagen eines PCB zu einem definierten Standard.



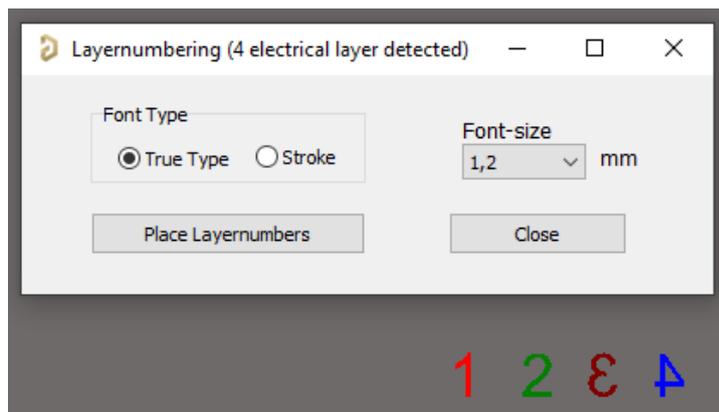
## Logo Placer

Mit diesem Skript können auf Bitmaps basierende Bilder als PCB-Logos platziert werden.



## Layer Numbering

Das Skript setzt einen PCB-String mit der entsprechenden Lagenummer auf die elektrischen Lagen.



## Schematic- and Layout Design Rule Check

Das Skript steuert verschiedene Testläufe und ordnet die Ergebnisse zu einem strukturierten Report.

Step	Kind	Details
LVS	[Changed Net Names]	[12V] in Schematic-Multivibrator.SchDoc <=> [<TEST>12V] in Layout-Multivibrator.PcbDoc
LVS	[Changed Net Names]	[GND] in Schematic-Multivibrator.SchDoc <=> [<TEST>GND] in Layout-Multivibrator.PcbDoc
LVS	[Changed Net Names]	[NetC1_1] in Schematic-Multivibrator.SchDoc <=> [<TEST>NetC1_1] in Layout-Multivibrator.PcbDoc
LVS	[Changed Net Names]	[NetC1_2] in Schematic-Multivibrator.SchDoc <=> [<TEST>NetC1_2] in Layout-Multivibrator.PcbDoc
LVS	[Changed Net Names]	[NetC2_1] in Schematic-Multivibrator.SchDoc <=> [<TEST>NetC2_1] in Layout-Multivibrator.PcbDoc
LVS	[Changed Net Names]	[NetC2_2] in Schematic-Multivibrator.SchDoc <=> [<TEST>NetC2_2] in Layout-Multivibrator.PcbDoc
LVS	[Extra Nets]	[<IGNORE DRC>] in Layout-Multivibrator.PcbDoc
LVS	[Extra Room Definitions]	[Room Schematic-Multivibrator (Scope=InComponentClass(Schematic-Multivibrator))] TopLayer] in Schematic-Multivibrator.SchDoc
DRC High Speed Rules	[Warning]	Only 0 High Speed Rule(s) found. You should have minimum 3 rules.
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Net <TEST>NetC2_2 Between Pad R4-1{(112.76mm,104.14mm) on Top Layer And Pad Q1-B{(116.31mm,115.8mm) on Top Layer
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Net <TEST>NetC2_2 Between Pad R4-1{(112.76mm,104.14mm) on Top Layer And Track {(114.03mm,102.87mm){(120.65mm,102.87mm) on Top Layer
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Net <TEST>12V Between Track {(111.76mm,115.57mm){(111.76mm,119.38mm) on Top Layer And Pad X1-1{(113.03mm,119.38mm) on Bottom Layer
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Net <TEST>GND Between Pad X1-2{(111.76mm,119.38mm) on Bottom Layer And Track {(113.03mm,118.053mm){(113.03mm,119.38mm) on Top Layer
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Split Plane (No Net) on Internal Plane 1 Dead Copper - Net Not Assigned.
DRC	[Un-Routed Net Constraint Violation]	Un-Routed Net Constraint: Split Plane (No Net) on Internal Plane 2 Dead Copper - Net Not Assigned.

## Layout Information

Das Skript erstellt einen Bericht zu dem Layoutzustandes des PCB.

Layout Information

Data

Sort Column: Unconnected (ASC/DESC) Connections = 14, connected = 10, unconnected = 4, diff. pair nets = 0, components = 9

Net	Pins	Connections	Connected	Unconnected
<TEST>NetC2_ 3	2	2	0	2
<TEST>12V 5	4	4	3	1
<TEST>GND 3	2	2	1	1
<TEST>NetC1_ 3	2	2	2	0
<TEST>NetC1_ 3	2	2	2	0
<TEST>NetC2_ 3	2	2	2	0

Selection Details (Double Click = Cross Probe)  
Un-Routed Net: <TEST>12V Between Track (111.76mm, 115.57mm)(111.76mm, 119.38mm) on Top Layer And Pad X1-1(113.03mm, 119.38mm) on Bottom Layer

## Assembly Support

Mit diesem Skript wird man bei handbestückten PCB's bei der Bestückung assistiert. Die Bauteile können per Crossprobing ermittelt- und als bestückt signiert werden.

Assembly Support

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Group by component

Variants: Variant B

VIEW:  Assembled,  Split by Side,  3D, Flip Board [F]

Done [Space] Skip [Esc] Stop Assembly

Name	Side	Designator	Status
CAP-0402-22n-50V-10%	Top	C1	✓
NPN-ZXTN2010Z	Top	Q2	✓
RES-0402-100K-63mW-	Top	R1	✓
RES-0402-1K-63mW-1%	Top	R2	✓
RES-0402-1K-63mW-1%	Top	R3	
RES-0402-100K-63mW-	Top	R4	
CON-Emi-214011	Bottom	X1	

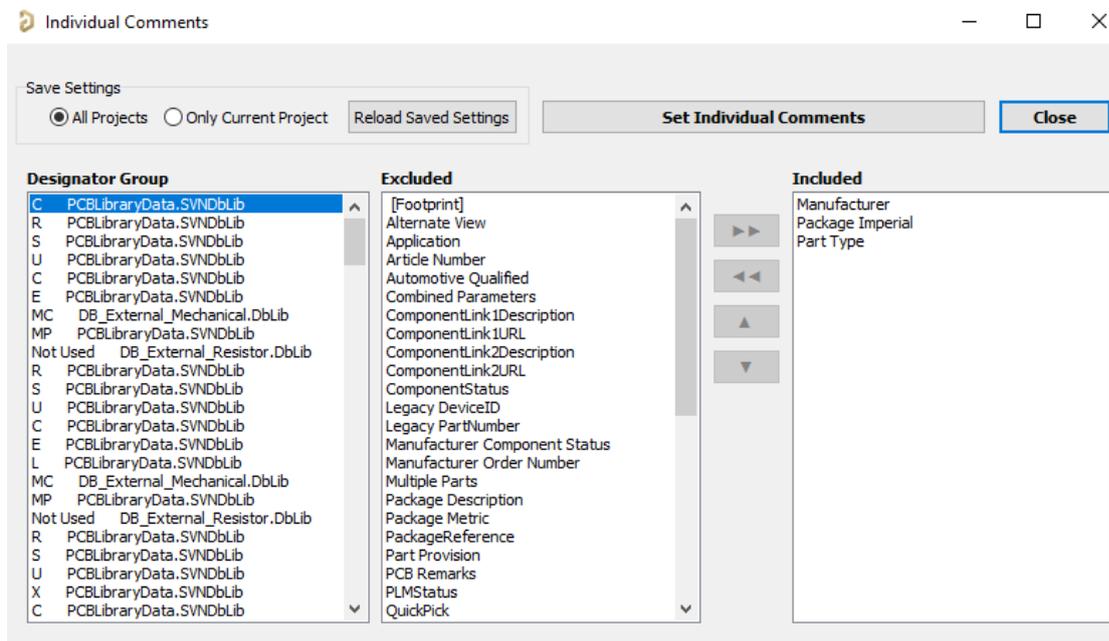
Component details: R3 = RES-0402-1K-63mW-1%

Name	Value
Comment	RES-0402-1K-63mW-1%
FullPar	RES-0402-1K-63mW-1%
ID	RES-000074
Kind	General
LibRef	Resistor
Netlist	@DESIGNATOR %1 %2 @VALUE
Package EIA	EIA 1005
Power	63mW
Price	Euro 0,05
Release-Status	Series Production

3D assembly view showing components R1, R2, R3, R4, C1, and Q2 on a PCB.

## Individual Comments

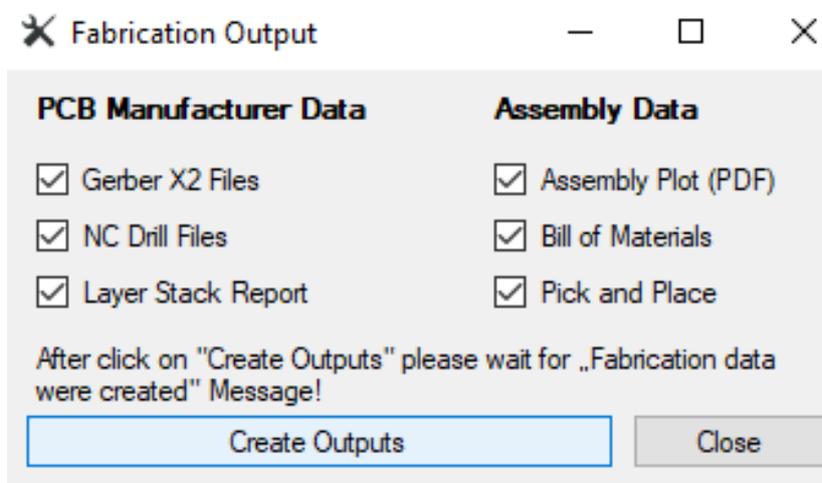
Mit diesem Skript können die PCB-Kommentare entsprechend der Bauteilklasse zusammengestellt werden.



## Allegro

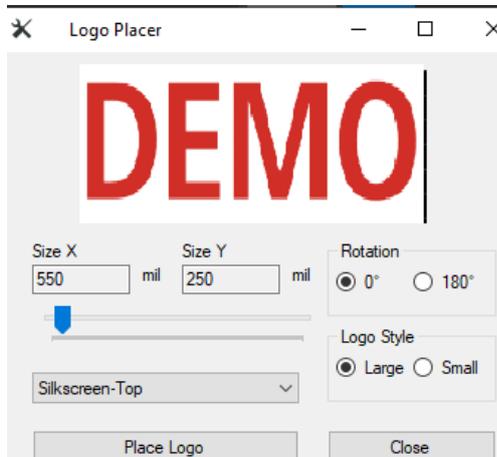
### One Click Documentaion

Das Skript erstellt die komplette Fertigungsdaten und Dokumentation zu einer bestückten Leiterplatte.



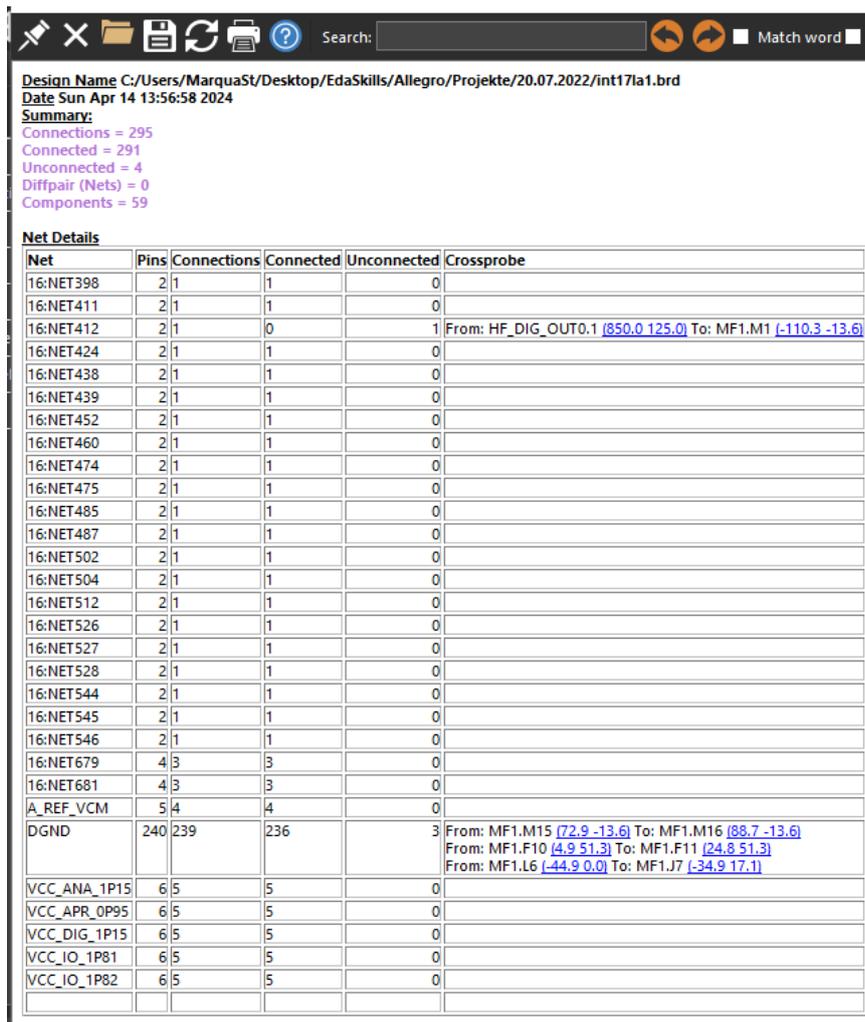
## Logo Placer

Mit diesem Skript können auf Bitmaps basierende Bilder als PCB-Logos platziert werden.



## Layout Information

Das Skript erstellt einen Bericht zu dem Layoutzustandes des PCB.



**Design Name** C:/Users/MarquasT/Desktop/EdaSkills/Allegro/Projekte/20.07.2022/int171a1.brd  
**Date** Sun Apr 14 13:56:58 2024  
**Summary:**  
Connections = 295  
Connected = 291  
Unconnected = 4  
Diffpair (Nets) = 0  
Components = 59

**Net Details**

Net	Pins	Connections	Connected	Unconnected	Crossprobe
16:NET398	2	1	1	0	
16:NET411	2	1	1	0	
16:NET412	2	1	0	1	From: HF_DIG_OUT0.1 (850.0 125.0) To: MF1.M1 (-110.3 -13.6)
16:NET424	2	1	1	0	
16:NET438	2	1	1	0	
16:NET439	2	1	1	0	
16:NET452	2	1	1	0	
16:NET460	2	1	1	0	
16:NET474	2	1	1	0	
16:NET475	2	1	1	0	
16:NET485	2	1	1	0	
16:NET487	2	1	1	0	
16:NET502	2	1	1	0	
16:NET504	2	1	1	0	
16:NET512	2	1	1	0	
16:NET526	2	1	1	0	
16:NET527	2	1	1	0	
16:NET528	2	1	1	0	
16:NET544	2	1	1	0	
16:NET545	2	1	1	0	
16:NET546	2	1	1	0	
16:NET679	4	3	3	0	
16:NET681	4	3	3	0	
A_REF_VCM	5	4	4	0	
DGND	240	239	236	3	From: MF1.M15 (72.9 -13.6) To: MF1.M16 (88.7 -13.6) From: MF1.F10 (4.9 51.3) To: MF1.F11 (24.8 51.3) From: MF1.L6 (-44.9 0.0) To: MF1.J7 (-34.9 17.1)
VCC_ANA_1P15	6	5	5	0	
VCC_APR_OP95	6	5	5	0	
VCC_DIG_1P15	6	5	5	0	
VCC_IO_1P81	6	5	5	0	
VCC_IO_1P82	6	5	5	0	